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IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A method for compressing output data ~~is~~ comprising:

writing a first data having a first number of bits [[in]] into an address of a core cell region;

reading the first data of the first number of bits written in the address as read data having the first number of bits;

comparing the first data and the read data by dividing each of the first data and the read data into an upper portion having a second number of bits and a lower portion having a remaining number of bits; and

generating a 1-bit compressed data for each of the upper portion and the lower portion with information indicating whether a failure is present.

2. (Currently amended) A method for compressing output data comprising:

reading a first data from a core cell region and prefetching the first data having a first number of bits in a normal mode;

writing the first data of the first number of bits [[in]] into an address of the core cell region in a test mode;

reading the first data written [[in]] into the address of the core cell region and prefetching the read data;

comparing the first data and the read data by dividing each of the first data and the read data into an upper portion having a second number of bits and a lower portion having a remaining number of bits; and

compressing a result from the comparing to generate a compressed data with information indicating whether a failure is present;

selecting a selected data from the prefetched first data in a normal mode and the compressed data in a test mode;

shifting the selected data at an ascending edge and a descending edge of a clock signal and outputting the selected data serially via one or more output pads in a normal mode;

shifting the selected data at an ascending edge and a descending edge of the clock signal and outputting the selected data serially via one of the one or more output pads in a test mode

3. (Currently amended) The method for compressing output data as in claim 2, wherein

the first number of bits associated with the prefetched first data, first data, and the read data is 8;

the second number of bits associated with the upper portion is 4;

the remaining number of bits associated with the lower portion is 4; and

the compressed data is a 1-bit signal.

4. (Currently amended) A packet command driving type memory device comprising:

a read data comparing part capable of receiving a first data and a read data from a core cell region, both the first data and the read data having a first number of bits, comparing the first data with the read data, and generating a compressed data having a second number of bits;

a data input/output part capable of transforming the compressed data and the read data to produce more than one data ~~parts~~ part;

an interface part capable of serially outputting the data parts from the data input/output part in a packet form via an output pad.

5. (Previously presented) The packet command driving type memory device as in claim 4, wherein

the first number of bits associated with the first data and the read data is 8;

the first data and the read data are divided into, during said comparing, an upper 4-bit portion and a lower 4-bit portion;

the second number of bits associated with the compressed data is 2 bits, the read data comparing part compressing the upper 4-bit portions of the first data and the read data into a first 1-bit signal of the compressed data and the lower 4-bit portions of the first data and the read data into a second 1-bit signal of the compressed data; and

the data parts include an even-bit data part and an odd-bit data part.

6. (Previously presented) The packet command driving type memory device as in claim 4, wherein the read data comparing part comprises:

plurality of comparators, each of which capable of receiving and comparing corresponding portions of the first data and the read data to generate a 1-bit compressed data indicating whether a failure is present; and

a selecting means capable of selecting the read data in a normal mode[[,]] and the compressed data generated by one of the plurality of comparators in a test mode.

7. (Currently amended) The packet command driving type memory device as in claim 6, wherein each of the plurality of comparators comprises:

a first comparing means capable of receiving a first bit of a 4-bit portion of the first data and a first bit of a 4-bit portion of the read data and comparing the received two first bits to generate a first 1-bit comparing signal;

a second comparing means capable of receiving a second bit of the 4-bit portion of the first data and a second bit of the 4-bit portion of the read data and comparing the received two second bits to generate a second 1-bit comparing signal;

a third comparing means capable of receiving a third bit of the 4-bit portion of the first data and a third bit of the 4-bit portion of the read data and comparing the received two third bits to generate a third 1-bit comparing signal;

a fourth comparing means capable of receiving a fourth bit of the 4-bit portion of the first data and a fourth bit of the 4-bit portion of the read data and comparing the received two fourth bits to generate a fourth 1-bit comparing signal; and

a generating means capable of receiving the first, the second, the third, and the fourth comparing signals and producing the 1-bit compressed data.

8. (Currently amended) The packet command driving type memory device as in claim 7, wherein each of the first, the second, the third, and the fourth comparing means comprises:

a first NAND GATE capable of receiving a 1-bit signal of the first data;

a second NAND GATE capable of receiving a corresponding 1-bit signal of the read data;

a third NAND GATE capable of receiving outputs of the first and the second NAND GATE;

a first and a second NMOS transistor having gates and drains receiving the outputs of the first and the second NAND GATE;

a first and a second PMOS transistor connected in series between a power voltage and a source of the first and the second NMOS transistors, having gates to receive the outputs of the first and the second NAND GATE;

a third PMOS transistor having a gate to receive an output of the third NAND GATE and a source to receive a power voltage and ~~drains~~ a drain connected between sources of the first and the second NMOS transistors and a drain ~~drains~~ of the ~~first and the~~ second PMOS transistor; wherein

the first, the second, the third, and the fourth comparing signals are generated via sources of the first and the second NMOS transistors and drains of the first to the third PMOS transistors.

9. (Previously presented) The packet command driving type memory device as in claim 7, wherein the generating means comprises a fourth NAND GATE receiving the first, the second, the third, and the fourth comparing signals as input and generating the 1-bit compressed data as output.

10. (Previously presented) A packet command driving type memory device comprising:

plurality of comparators for receiving and comparing 8-bit data read from a core cell region and generating compressed data, wherein each of the comparators is capable of

receiving 4 bits of an 8-bit first data and 4 bits of an 8-bit prefetched data read from an address of the core cell region where the first data is written, the received 4 bits of the first data being one of a 4-bit upper portion and a 4-bit lower portion of the first data and the received 4 bits of the prefetched data being one of a 4-bit upper portion and a 4-bit lower portion of the prefetched data,

comparing the 4 bits of the first data and the 4 bits of the prefetched data in a test mode, and

generating a 1-bit compressed data based on a result of the comparing with information indicating whether a failure is present; and

a selecting means capable of selecting the 8-bit prefetched data in a normal mode and the compressed data from the plurality of comparators in the test mode.

11. (Previously presented) A packet command driving type memory device comprising:

a read data comparing part having a plurality of comparators capable of receiving an 8-bit first data and an 8-bit prefetched data read from an address of a core cell region where the first data is written,

comparing the received first data with the prefetched data by comparing, via each of the plurality of comparators, corresponding upper and lower 4 bits of the 8-bit first data and the 8-bit prefetched data in a test mode, and

generating, by each of the plurality of comparators, a 1-bit compressed data for each of the comparing performed based on corresponding 4 bits portions of the first data and the prefetched data,

selecting a selected data from the 8-bit prefetched data in a normal mode and the compressed data from the plurality of comparators in a test mode;

a data input/output part capable of transforming the selected data into more than one data parts; and

an interface part capable of serially outputting the data parts of the selected data from the data input/output part.